

equations for any cell (basic atom cell, higher-order cell, etc.) into the cell, such that when the cell is compiled, the desired resulting cell is created. (For example, a standard C5_235 cell may be turned into a transistor cell.)

Furthermore, in one particular embodiment of the invention, the system also includes a cleansheet file, which desirably is a spreadsheet that contains current design rules for the plurality of cells, such that values for the global variables of the global file are derived therefrom. In this embodiment, desirably an extract mechanism, such as a computer program, is utilized to update values for the global variables of the global file from the current design rules of the clean sheet file. If a design is performed with well construct global and local files, then the design can parametrically adjust itself to any new set of design rules without a designer having to manually redraw a single structure.

The present invention includes computerized systems, methods, structures, computer-readable media, and computers of varying scope. In one embodiment of the invention, the invention is implemented in conjunction with Design Framework II (DF2) software available from Cadence Design Systems, Inc. In addition to the aspects and advantages of the present invention described in this summary, further aspects and advantages of the invention will become apparent by reference to the drawings and by reading the detailed description that follows.

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BRIEF DESCRIPTION OF THE DRAWINGS

FIGs. 1(a), 1(b), and 1(c) show diagrams of a representative hierarchy of a semiconductor structure, in accordance with which embodiments of the invention may be implemented;

FIG. 2 shows a diagram of a computer in conjunction with which an embodiments of the invention may be implemented;

FIG. 3 shows a diagram of a semiconductor memory that may be tested with a semiconductor test structure hierarchically designed in conjunction with which embodiments of the invention may be utilized (although the invention is not so